ASP-DAC 2014 Advance Program

2014 19th Asia and South Pacific Design Automation Conference (ASP-DAC)
Date: Jan 20-23, 2014
Place: Suntec, Singapore

Highlights

Opening and Keynote I

Tuesday, January 21, 2014, 08:30 – 10:00

Ivo Bolsens (Senior VP & CTO, Xilinx, U.S.A.) "*All Programmable SOC FPGA for Networking and Computing in Big Data Infrastructure*"

Keynote II

Wednesday, January 22, 2014, 08:30 – 09:30

Georges Gielen (Katholieke Univ. Leuven, Belgium) "*Designing Analog Functions without Analog Transistors*"

Keynote III

Thursday, January 23, 2014, 08:30 – 09:30

Kaushik Roy (Purdue Univ., U.S.A.) "*Beyond Charge-Based Computing"*

Banquet Keynote

Wednesday, January 22, 2014, 18:30 – 21:00

Ulf Schneider (Managing Director, Lantiq Asia Pacific Pte/President, SSIA, Singapore) "*The Art of Innovation - How Singapore Will Continue to Drive the Progress in Semiconductor Technologies"*

Special Sessions

1A: (Presentation + Poster Discussion) University Design Contest
Tuesday, January 21, 2014, 10:40 – 12:20

1S: (Invited Talks) Normally-Off Computing: Towards Zero Stand-by Power Management
Tuesday, January 21, 2014, 10:40 – 12:20

2S: (Invited Talks) EDA for Energy
Tuesday, January 21, 2014, 13:50 – 15:30

3S: (Invited Talks) Neuron Inspired Computing using Nanotechnology
Tuesday, January 21, 2014, 15:50 – 17:30

4S: (Invited Talks) Design Automation Methods for Highly-Complex Multimedia Systems
Wednesday, January 22, 2014, 10:10 – 12:15

5S: (Invited Talks) Billion Chips of Trillion Transistors
Wednesday, January 22, 2014, 13:50 – 15:30

6S: (Invited Talks) Overcoming Major Silicon Bottlenecks: Variability, Reliability, Validation, and Debug
Wednesday, January 22, 2014, 15:50 – 17:30

7S: (Invited Talks) Brain Like Computing: Modelling, Technology, and Architecture
Thursday, January 23, 2014, 10:10 – 12:15

8S: (Invited Talks) Design Flow for Integrated Circuits using Magnetic Tunnel Junction Switched by Spin Orbit Torque
Thursday, January 23, 2014, 13:50 – 15:30

9S: (Invited Talks) The Role of Photons in Harming or Increasing Security
Thursday, January 23, 2014, 15:50 – 17:30

Tutorials

ASP-DAC has changed the format for the tutorials. Instead of full-day, in-depth tutorials, participants can choose two 3-hour tutorials – one in the morning session and one in the afternoon. For each session, four options are available – two in the physical-design (PD) domain and two in the system-design (SD) domain.

Tutorial-PD1: Energy-Efficient Datacenters
Monday, January 20, 2014, 09:00 – 12:00
Speaker:
Massoud Pedram (Univ. of Southern California, U.S.A.)

Tutorial-PD2: Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyber-Physical System Integration
Monday, January 20, 2014, 14:00 – 17:00
Speakers:
Tsung-Yi Ho (National Cheng Kung Univ, Taiwan)
Krishnendu Chakrabarty (Duke Univ., U.S.A.)

Tutorial-PD3: On Variability and Reliability; Dynamic Margining and Low Power
Monday, January 20, 2014, 09:00 – 12:00
Speakers:
Fadi Kurdahi (Univ. of California, Irvine, U.S.A.)
Greg Taylor (Intel Research Lab, U.S.A.)
Ahmed Eltawil (Univ. of California, Irvine, U.S.A.)
Amin Khajeh (Intel Research Lab, U.S.A.)

Tutorial-PD4: Architecture Level Thermal Modeling, Prediction and Management for Multi-Core and 3D Microprocessors
Monday, January 20, 2014, 14:00 – 17:00
Speakers:
Sheldon Tan (Univ. of California, Riverside, U.S.A.)
Hai Wang (Univ. of Electronic Science and Technology , China)

Tutorial-SD1: High-Level Specifications to Cope with Design Complexity
Monday, January 20, 2014, 14:00 – 17:00
Speakers:
Gunar Schirner (Northeastern Univ., U.S.A.)
Wolfgang Müller (Univ. of Paderborn, Germany)
Eugenio Villar (Univ. of Cantabria, Spain)
Rainer Dömer (Univ. of California, Irvine, U.S.A.)

Tutorial-SD2: Many-core and Heterogeneous System-Level Verification Methodology
Monday, January 20, 2014, 09:00 – 12:00
Speakers:
Alex Goryachev (IBM Research - Haifa, Israel)
Ronny Morad (IBM Research - Haifa, Israel)

Tutorial-SD3: The Formal Specification Level: Bridging the Gap between the Spec and its Implementation
Monday, January 20, 2014, 14:00 – 17:00
Speakers:
Robert Wille (Univ. of Bremen, Germany)
Rainer Findenig (Intel Mobile Communications, Austria)
Rolf Drechsler (DFKI GmbH, Germany)

Tutorial-SD4: High-Level Synthesis for Low-Power Design
Monday, January 20, 2014, 09:00 – 12:00
Speakers:
Zhiru Zhang (Cornell Univ., U.S.A.)
Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)

Monday, January 20, 2014

NEW!! ASP-DAC has changed the format for the tutorials. Instead of full-day, in-depth tutorials, participants can choose two 3-hour tutorials – one in the morning session and one in the afternoon. For each session, four options are available – two in the physical-design (PD) domain and two in the system-design (SD) domain.

Registration (08:00 –)				
09:00 10:20* – 10:40 12:00	**Tutorial-PD1: Energy-Efficient Datacenters** Organizer: Massoud Pedram (Univ. of Southern California, U.S.A) Speaker: Massoud Pedram (Univ. of Southern California, U.S.A.)	**Tutorial-SD2: Many-core and Heterogeneous System-Level Verification Methodology** Organizer: Ronny Morad (IBM Research, Haifa, Israel) Speakers: Alex Goryachev (IBM Research, Haifa ,Israel) Ronny Morad (IBM Research, Haifa, Israel)	**Tutorial-PD3: On Variability and Reliability; Dynamic Margining and Low Power** Organizer: Fadi Kurdahi (Univ. of California, Irvine, U.S.A.) Speakers: Fadi Kurdahi (Univ. of California, Irvine, U.S.A.) Greg Taylor (Intel Research Lab, U.S.A) Ahmed Eltawil (Univ. of California, Irvine, U.S.A.) Amin Khajeh (Intel Research Lab, U.S.A.)	**Tutorial-SD4: High-Level Synthesis for Low-Power Design** Organizer: Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.) Speakers: Zhiru Zhang (Cornell Univ., U.S.A.) Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)
Lunch Break (12:00 – 14:00)				
14:00 15:20* – 15:40 17:00	**Tutorial-SD1: High-Level Specifications to Cope with Design Complexity** Organizer: Gunar Schirner (Northeastern Univ., U.S.A.) Speakers: Gunar Schirner (Northeastern Univ., U.S.A.) Wolfgang Müller (Univ. of Paderborn/C-LAB) Eugenio Villar (Univ. of Cantabria, Spain) Rainer Dömer (Univ. of California, Irvine, U.S.A.)	**Tutorial-PD2: Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyber-Physical System Integration** Organizer: Tsung-Yi Ho (National Cheng Kung Univ, Taiwan) Speakers: Tsung-Yi Ho (National Cheng Kung Univ, Taiwan) Krishnendu Chakrabarty (Duke Univ., U.S.A.)	**Tutorial-SD3: The Formal Specification Level: Bridging the Gap between the Spec and its Implementation** Organizer: Robert Wille (Univ. of Bremen, Germany) Speakers: Robert Wille (Univ. of Bremen, Germany) Rainer Findenig (Intel Mobile Communications, Austria) Rolf Drechsler (DFKI GmbH, Germany)	**Tutorial-PD4: Architecture Level Thermal Modeling, Prediction and Management for Multi-Core and 3D Microprocessors** Organizer: Sheldon Tan (Univ. of California, Riverside, U.S.A.) Speakers: Sheldon Tan (Univ. of California, Riverside, U.S.A.) Hai Wang (Univ. of Electronic Science and Technology, China)
Welcome Reception+ (18:00 – 20:00)				

* Tea refreshment will be provided

+ Please refer to the website for more information

Tuesday, January 21, 2014

Registration (08:00 –)

08:30 – 10:00

1K: Opening & Keynote I

Chairs: Yong Lian, Yajun Ha (National Univ. of Singapore, Singapore)

Ivo Bolsens (Senior VP & CTO, Xilinx, U.S.A.) "*All Programmable SOC FPGA for Networking and Computing in Big Data Infrastructure*"

Coffee Break (10:00 – 10:40)

10:40 – 12:20

1S: Special Session: Normally-Off Computing: Towards Zero Stand-by Power Management

Organizer: Hiroshi Nakamura (Univ. of Tokyo, Japan)

1S-1: Hiroshi Nakamura, Takashi Nakada, Shinobu Miwa (Univ. of Tokyo, Japan) "*Normally-Off Computing Project : Challenges and Opportunities*"

1S-2: Shinobu Fujita, Kumiko Nomura, Hiroki Noguchi, Susumu Takeda, Keiko Abe (Toshiba Corp., Japan) "*Novel Nonvolatile Memory Hierarchies to Realize "Normally-Off Mobile Processors*""

1S-3: Masanori Hayashikoshi, Yohei Sato, Hiroshi Ueki, Hiroyuki Kawai, Toru Shimizu (Renesas Electronics Corp., Japan) "*Normally-Off MCU Architecture for Low-power Sensor Node*"

1S-4: Shintaro Izumi, Hiroshi Kawaguchi, Yoshimoto Masahiko (Kobe Univ., Japan), Yoshikazu Fujimori (Rohm, Japan) "*Normally-Off Technologies for Healthcare Appliance*"

1A: (Presentation + Poster Discussion) University Design Contest

Chair: Chun Huat Heng (National Univ. of Singapore, Singapore)

(The authors and the titles of the presentations are listed in the next page)

1B: Planning and Placement for Design Closure and Manufacturability

Chairs: Shigetoshi Nakatake (Univ. of Kitakyushu, Japan), Hung-Ming Chen (National Chiao Tung Univ., Taiwan)

1B-1: Shuai Li, Cheng-Kok Koh (Purdue Univ., U.S.A.) "*Analytical Placement of Mixed-Size Circuits for Better Detailed-Routability*"

1B-2: Seongbo Shim, Yoojong Lee, Youngsoo Shin (KAIST, Republic of Korea) "*Lithographic Defect Aware Placement Using Compact Standard Cells Without Inter-Cell Margin*"

1B-3: Johann Knechtel (Dresden Univ. of Tech., Germany), Evangeline F. Y. Young (Chinese Univ. of Hong Kong, Hong Kong), Jens Lienig (Dresden Univ. of Tech., Germany) "*Structural Planning of 3D-IC Interconnects by Block Alignment*"

1B-4: Rani Ghaida (Global Foundries, U.S.A.), Yasmine Badr, Mukul Gupta (Univ. of California, Los Angeles, U.S.A.), Ning Jin (Global Foundries, U.S.A.), Puneet Gupta (Univ. of California, Los Angeles, U.S.A.) "*Comprehensive Die-Level Assessment of Design Rules and Layouts*"

1C: Circuit, Architecture, and System for Emerging Technologies

Chairs: Hai (Helen) Li (Univ. of Pittsburgh, U.S.A.), Danghui Wang (Northwestern Polytechnical Univ., China)

1C-1: Mengjie Mao (Univ. of Pittsburgh, U.S.A.), Guangyu Sun (Peking Univ., China), Yong Li, Alex K. Jones, Yiran Chen (Univ. of Pittsburgh, U.S.A.) "*Prefetching Techniques for STT-RAM Based Last-Level Cache in CMP Systems*"

1C-2: Sven Tenzing Choden Konigsmark, Leslie Hwang, Deming Chen, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.) "*CNPUF: A Carbon Nanotube-based Physically Unclonable Function for Secure Low-Energy Hardware Design*"

1C-3: Hossam Sarhan, Sebastien Thuries, Olivier Billoint, Fabien Clermidy (CEA-LETI, France) "*3DCoB: A New Design Approach for Monolithic 3D Integrated Circuits*"

1C-4: Yuko Hara-Azumi (Nara Inst. of Science and Tech./JST, PRESTO, Japan), Masaya Kunimoto, Yasuhiko Nakashima (NAIST, Japan) "*Emulator-Oriented Tiny Processors for Unreliable Post-Silicon Devices: A Case Study*"

Lunch Break/University Design Contest Discussion (12:20 – 13:50)

Tuesday, January 21, 2014

10:40

1A: (Presentation + Poster Discussion) University Design Contest

Chair: Chun Huat Heng (National Univ. of Singapore, Singapore)

1A-1: Wei Deng, Ahmed Musa, Teerachot Siriburanon, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) "*A Dual-Loop Injection-Locked PLL with All-Digital Background Calibration System for On-Chip Clock Generation*"

1A-2: Sho Ikeda, Tatsuya Kamimura, Sangyeop Lee, Hiroyuki Ito, Noboru Ishihara, Kazuya Masu (Tokyo Inst. of Tech., Japan) "*A 950μW 5.5-GHz Low Voltage PLL with Digitally-Calibrated ILFD and Linearized Varactor*"

1A-3: Teerachot Siriburanon, Wei Deng, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan) "*A Swing-Enhanced Current-Reuse Class-C VCO with Dynamic Bias Control Circuits*"

1A-4: Xiaojun Bi (National Univ. of Singapore/Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Yongxin Guo (National Univ. of Singapore, Singapore), M. Annamalai Arasu (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), M. S. Zhang (National Univ. of Singapore, Singapore), Yong Zhong Xiong, Minkyu Je (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), "*Design of A High-Performance Millimeter-Wave Amplifier Using Specific Modeling*"

1A-5: Zheng Song, Nan Qi, Baoyong Chi, Zhihua Wang (Tsinghua Univ., China) "*A Multi-Mode Reconfigurable Analog Baseband with I/Q Calibration for GNSS Receivers*"

1A-6: Kentaro Yoshioka, Akira Shikata, Ryota Sekimoto, Tadahiro Kuroda, Hiroki Ishikuro (Keio Univ., Japan) "*An 8b Extremely Area Efficient Threshold Configuring SAR ADC with Source Voltage Shifting Technique*"

1A-7: Jungmoon Kim, Chulwoo Kim (Korea Univ., Republic of Korea) "*A Single-Inductor 8-Channel Output DC-DC Boost Converter with Time-Limited Power Distribution Control and Single Shared Hysteresis Comparator*"

1A-8: Jungmoon Kim, Minseob Kim, Junwon Jung, Heejun Kim, Chulwoo Kim (Korea Univ., Republic of Korea) "*A DC-DC Boost Converter with Variation Tolerant MPPT Technique and Efficient ZCS Circuit for Thermoelectric Energy Harvesting Applications*"

1A-9: Hoyoung Yoo, Youngjoo Lee, In-Cheol Park (KAIST, Republic of Korea) "*7.3 Gb/s Universal BCH Encoder and Decoder for SSD Controllers*"

1A-10: Won-Tae Kim, Hui-Sung Jeong, Gwang-Ho Lee, Tae-Hwan Kim (Korea Aerospace Univ., Republic of Korea) "*A High-Speed and Low-Complexity Lens Distortion Correction Processor for Wide-Angle Cameras*"

12:20

Lunch Break/University Design Contest Discussion (12:20 – 13:50)

Tuesday, January 21, 2014

13:50	**2S: Special Session: EDA for Energy** Organizers: Fadi Kurdahi (Univ. of California, Irvine, U.S.A.), Sani Nassif (IBM, U.S.A.), Mohammad Al Faruque (Univ. of California, Irvine, U.S.A.) **2S-1:** Sani Nassif, Gi-Joon Nam, Jerry Hayes (IBM, U.S.A.), Sani Fakhouri (EPE / UCI, U.S.A.) "*Applying VLSI EDA to Energy Distribution System Design*" **2S-2:** Mohammad Abdullah Al Faruque, Fereidoun Ahourai (Univ. of California, Irvine, U.S.A.) "*A Model-Based Design of Cyber-Physical Energy Systems*" **2S-3:** Hao Chen, Michael Caramanis, Ayse K. Coskun, (Boston Univ., U.S.A.) "*The Data Center as a Grid Load Stabilizer*"	**2A: Distributed and Mixed-Criticality Real-Time Systems** Chairs: Nan Guan (Northeastern Univ., China), Philip Brisk (Univ. of California, Riverside, U.S.A.) **2A-1:** Hany Kashif, Hiren D. Patel (Univ. of Waterloo, Canada) "*Bounding Buffer Space Requirements for Real-Time Priority-Aware Networks*" **2A-2:** Licong Zhang, Dip Goswami, Reinhard Schneider, Samarjit Chakraborty (TU Munich, Germany) "*Task- and Network-Level Schedule Co-Synthesis of Ethernet-Based Time-Triggered Systems*" **2A-3:** Pengcheng Huang, Georgia Giannopoulou, Nikolay Stoimenov, Lothar Thiele (ETH Zurich, Switzerland) "*Service Adaptions for Mixed-Criticality Systems*" **2A-4:** Xiaotong Cui, Jun Zhang, Kaijie Wu, Edwin Sha (Chongqing Univ., China) "*Efficient Feasibility Analysis of DAG Scheduling with Real-Time Constraints in the Presence of Faults*"	**2B: Advanced Patterning for Advanced Layout** Chairs: Martin Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.), Shigeki Nojima (Toshiba, Japan) **2B-1:** Chris Chu (Iowa State Univ., U.S.A.), Wai-Kei Mak (National Tsing Hua Univ., Taiwan) "*Flexible Packed Stencil Design with Multiple Shaping Apertures for E-Beam Lithography*" **2B-2:** Jhih-Rong Gao, Bei Yu, David Z. Pan (Univ. of Texas, Austin, U.S.A.) "*Self-Aligned Double Patterning Layout Decomposition with Complementary E-Beam Lithography*" **2B-3:** Sambuddha Bhattacharya, Subramanian Rajagopalan, Shabbir H Batterywala (Synopsys India Pvt., India) "*Fixing Double Patterning Violations with Look-Ahead*" **2B-4:** Abde Ali Kagalwalla (Univ. of California, Los Angeles, U.S.A.), Michael Lam, Kostas Adam (Mentor Graphics, U.S.A.), Puneet Gupta (Univ. of California, Los Angeles, U.S.A.) "*EUV-CDA: Pattern Shift Aware Critical Density Analysis for EUV Mask Layouts*"	**2C: Timing-Driven Design, Modeling, and Optimization** Chairs: Mango Chia-Tso Chao (National Chiao Tung Univ., Taiwan), Tai-Chen Chen (National Central Univ., Taiwan) **2C-1:** Xiaoming Chen, Yu Wang (Tsinghua Univ., China), Yu Cao (Arizona State Univ., U.S.A.), Huazhong Yang (Tsinghua Univ., China) "*Statistical Analysis of Random Telegraph Noise in Digital Circuits*" **2C-2:** Tiansong Cui, Yanzhi Wang, Xue Lin, Shahin Nazarian, Massoud Pedram (Univ. of Southern California, U.S.A.) "*Semi-Analytical Current Source Modeling of FinFET Devices Operating in Near/Sub-Threshold Regime with Independent Gate Control and Considering Process Variation*" **2C-3:** Yukihide Kohira (Univ. of Aizu, Japan), Atsushi Takahashi (Tokyo Inst. of Tech., Japan) "*2-SAT Based Linear Time Optimum Two-Domain Clock Skew Scheduling*" **2C-4:** Insup Shin (KAIST, Republic of Korea), Jae-Joon Kim (POSTECH, Republic of Korea), Youngsoo Shin (KAIST, Republic of Korea) "*Power Minimization of Pipeline Architecture through 1-Cycle Error Correction and Voltage Scaling*"
15:30				
Coffee Break (15:30 – 15:50)				

Tuesday, January 21, 2014

15:50

17:30

3S: Special Session: Neuron Inspired Computing using Nanotechnology (Tentative)

Organizers: Kevin Cao (Arizona State Univ., U.S.A.), Sarma Vrudhula (Arizona State Univ., U.S.A.)

3S-1: Takashi Morie, Haichao Liang, Yilai Sun, Takashi Tohara (Kyushu Inst. of Tech., Japan), Makoto Igarashi, Seiji Samukawa (Tohoku Univ., Japan) "*A Silicon Nanodisk Array Structure Realizing Synaptic Response of Spiking Neuron Models with Noise*"

3S-2: Hao Yu, Yuhao Wang, Shuai Chen, Wei Fei (Nanyang Technological Univ., Singapore), Chuliang Weng, Junfeng Zhao, Zhulin Wei (Huawei Shannon Laboratory, China) "*Energy Efficient In-memory Machine Learning for Data Intensive Image-processing by Non-volatile Domain-Wall Memory*"

3S-3: Louis Scheffer (Howard Hughes Medical Institute, U.S.A.) "*Lessons from the Neurons Themselves*"

3A: Synthesis and Exploration Techniques for Computing Platforms

Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), Kyle Rupnow (Nanyang Technological Univ.)

3A-1: Zidong Du (State Key Laboratory of Computer Architecture, Institute of Computing Technology, China Academy of Sciences, China), Avinash Lingamneni (Rice Univ., U.S.A.), Yunji Chen (State Key Laboratory of Computer Architecture, Institute of Computing Technology, China Academy of Sciences, China), Krishna Palem (Rice Univ., U.S.A.), Olivier Temam (INRIA, France), Chengyong Wu (State Key Laboratory of Computer Architecture, Institute of Computing Technology, China Academy of Sciences, China) "*Leveraging the Error Resilience of Machine-Learning Applications for Designing Highly Energy Efficient Accelerators*"

3A-2: Fabian Oboril, Mehdi Tahoori (KIT, Germany) "*ArISE: Aging-Aware Instruction Set Encoding for Lifetime Improvement*"

3A-3: Giovanni Mariani (Univ. della Svizzera Italiana - ALaRI, Switzerland), Gianluca Palermo (Politecnico di Milano - DEIB, Italy), Roel Meeuws, Vlad-Mihai Sima (Delft Technical Univ., Netherlands), Cristina Silvano (Politecnico di Milano - DEIB, Italy), Koen Bertels (Delft Technical Univ., Netherlands) "*DRuiD: Designing Reconfigurable Architectures with Decision-Making Support*"

3A-4: Hui Huang (Univ. of California, Los Angeles, U.S.A.), Taemin Kim, Yatin Hoskote (Intel Labs, U.S.A.) "*Edit Distance Based Instruction Merging Technique to Improve Flexibility of Custom Instructions Toward Flexible Accelerator Design*"

3B: Advances in Microfluidic Biochips

Chairs: Tsung-Yi Ho (National Cheng Kung Univ., Taiwan), Juinn-Dar Huang (National Chiao Tung Univ., Taiwan)

3B-1: Trung Anh Dinh, Shigeru Yamashita (Ritsumeikan Univ., Japan), Tsung-Yi Ho (National Cheng Kung Univ., Taiwan) "*A Network-Flow-Based Optimal Sample Preparation Algorithm for Digital Microfluidic Biochips*"

3B-2: Johnathan Fiske, Daniel Grissom, Philip Brisk (Univ. of California, Riverside, U.S.A.) "*Exploring Speed and Energy Tradeoffs in Droplet Transport for Digital Microfluidic Biochips*"

3B-3: Ho Chuen Jackson Yeung, Evangeline F.Y. Young (Chinese Univ. of Hong Kong, Hong Kong) "*General Purpose Cross-Referencing Microfluidic Biochip with Reduced Pin-Count*"

3B-4: Kai Hu (Duke Univ., U.S.A.), Tsung-Yi Ho (National Cheng Kung Univ., Taiwan), Krishnendu Chakrabarty (Duke Univ., U.S.A.) "*Wash Optimization for Cross-Contamination Removal in Flow-Based Microfluidic Biochips*"

3C: Advanced Modeling and Simulation Techniques for Analog/Mixed-Signal Circuits

Chairs: Hao Yu (Nanyang Technological Univ.), Shi Guoyong (Shanghai Jiao Tong Univ., China)

3C-1: Aadithya V. Karthik, Sayak Ray, Pierluigi Nuzzo, Alan Mishchenko, Robert Brayton, Jaijeet Roychowdhury (Univ. of California, Berkeley, U.S.A.) "*ABCD-NL: Approximating Continuous Non-Linear Dynamical Systems Using Purely Boolean Models for Analog/Mixed-Signal Verification*"

3C-2: Jun Tao, Ying-ChihWang, Minhee Jun, Xin Li, Rohit Negi, Tamal Mukherjee, Larry Pileggi (Carnegie Mellon Univ., U.S.A.) "*Toward Efficient Programming of Reconfigurable Radio Frequency (RF) Receivers*"

3C-3: Quan Chen, Wenhui Zhao, Ngai Wong (Univ. of Hong Kong, Hong Kong) "*Efficient Matrix Exponential Method Based on Extended Krylov Subspace for Transient Simulation of Large-Scale Linear Circuits*"

Wednesday, January 22, 2014

Registration (08:00 –)

08:30 – 09:30

2K: Keynote II

Chair: Nagisa Ishiura (Kwansei Gakuin Univ., Japan)

Georges Gielen (Katholieke Univ. Leuven, Belgium) "*Designing Analog Functions without Analog Transistors*"

Coffee Break (09:30 – 10:10)

10:10 – 12:15

4S: Special Session: Design Automation Methods for Highly-Complex Multimedia Systems

Organizer: Sri Parameswaran (Univ. of New South Wales, Australia)

4S-1: Jude Angelo Ambrose, Jorgen Peddersen (Univ. of New South Wales, Australia), Alvin Labios, Yusuke Yachide (Canon Information Systems Research Australia (CiSRA), Australia), Sri Parameswaran (Univ. of New South Wales, Australia) "*SDG2KPN: System Dependency Graph to Function-level KPN generation of Legacy Code for MPSoCs*"

4S-2: Muhammad Shafique, Jörg Henkel (Karlsruhe Inst. of Tech., Germany) "Low Power Design of the Next-Generation High Efficiency Video Coding"

4S-3: Kazutoshi Wakabayashi, Takeshi Takenaka, Hiroaki Inoue (NEC, Japan) *"Mapping Complex Algorithm into FPGA with High Level Synthesis*"

4S-4: Jihyun Ryoo, Kyuseung Han, Kiyoung Choi (Seoul National Univ., Republic of Korea) "*Leveraging Parallelism in the Presence of Control Flow on CGRAs*"

4A: System-Level Thermal and Power Optimization Techniques

Chairs: Yun (Eric) Liang (Peking Univ., China), Wengfai Wong (National Univ. of Singapore)

4A-1: Bagher Salami (Ferdowsi Univ. of Mashhad, Iran), Mohammadreza Baharani (Univ. of Tehran, Iran), Hamid Noori (Ferdowsi Univ. of Mashhad, Iran), Farhad Mehdipour (Kyushu Univ., Japan) "*Physical-Aware Task Migration Algorithm for Dynamic Thermal Management of SMT Multi-Core Processors*"

4A-2: Xiaohang Wang, Zhiming Li (Guangzhou Institute of Advanced Technology, CAS, China), Mei Yang, Yingtao Jiang (Univ. of Nevada, Las Vegas, U.S.A.), Masoud Daneshtalab (Univ. of Turku, Finland), Terrence Mak (Chinese Univ. of Hong Kong, China) "*Agile Frequency Scaling for Adaptive Power Allocation in Many-Core Systems Powered by Renewable Energy Sources*"

4A-3: Ioannis Stamelakos, Sotirios Xydis, Gianluca Palermo, Cristina Silvano (Politecnico di Milano, Italy) "*Variation Aware Voltage Island Formation for Power Efficient Near-Threshold Manycore Architectures*"

4A-4: Hiroyuki Usui, Jun Tanabe, Toru Sano, Hui Xu, Takashi Miyamori (Toshiba, Japan) "*An Evaluation of an Energy Efficient Many-Core SoC with Parallelized Face Detection*"

4A-5: Wei Jiang (Univ. of Electronic Science & Tech. of China, China), Ke Jiang (Linköping Univ., Sweden), Xia Zhang (Univ. of Electronic Science & Tech. of China, China), Yue Ma (Univ. of Notre Dame, U.S.A.) "*Energy Aware Real-Time Scheduling Policy with Guaranteed Security Protection*"

4B: Emerging Techniques for Future NoC

Chairs: Paul Bogdan (Univ. of Southern California, U.S.A.), Jiang Xu (HKUST)

4B-1: Zhiliang Qian (Hong Kong Univ. of Science and Tech., Hong Kong), Da-cheng Juan (Carnegie Mellon Univ., U.S.A.), Bogdan Paul (Univ. of Southern California, U.S.A.), Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong), Diana Marculescu, Radu Marculescu (Carnegie Mellon Univ., U.S.A.) "*A Comprehensive and Accurate Latency Model for Network-on-Chip Performance Analysis*"

4B-2: Georgios Faldamis (Cavium, U.S.A.), Weiwei Jiang (Columbia Univ., U.S.A.), Gennette Gill (D.E. Shaw Research, U.S.A.), Steven M. Nowick (Columbia Univ., U.S.A.) "*A Low-Latency Asynchronous Interconnection Network with Early Arbitration Resolution*"

4B-3: Alberto Ghiribaldi, Herve Tatenguem Fankem (Univ. of Ferrara, Italy), Federico Angiolini (iNoCs, Switzerland), Mikkel Stensgaard, Tobias Bjerregaard (Teklatech, Denmark), Davide Bertozzi (Univ. of Ferrara, Italy) "*A Vertically Integrated and Interoperable Multi-Vendor Synthesis Flow for Predictable NoC Design in Nanoscale Technologies*"

4B-4: Yuan Yao, Zhonghai Lu (Royal Inst. of Tech., Sweden) "*Fuzzy Flow Regulation for Network-on-Chip Based Chip Multiprocessors Systems*"

4B-5: Mohammad Fattah, Pasi Liljeberg, Juha Plosila, Hannu Tenhunen (Univ. of Turku, Finland) "*Adjustable Contiguity of Run-Time Task Allocation in Networked Many-Core Systems*"

4C: Emerging Applications

Chairs: Yu Wang (Tsinghua Univ., China), Dajiang Zhou (Waseda Univ., Japan)

4C-1: Xiaoxiao Liu, Yong Li, Yaojun Zhang, Alex K. Jones, Yiran Chen (Univ. of Pittsburgh, U.S.A.) "*STD-TLB: A STT-RAM-Based Dynamically-Configurable Translation Lookaside Buffer for GPU Architectures*"

4C-2: Boxun Li, Yuzhi Wang, Yu Wang (Tsinghua Univ., China), Yiran Chen (Univ. of Pittsburgh, U.S.A.), Huazhong Yang (Tsinghua Univ., China) "*Training Itself: Mixed-Signal Training Acceleration for Memristor-Based Neural Network*"

4C-3: Jia Zhu, Zhenyu Liu, Dongsheng Wang (Tsinghua Univ., China), Qingrui Han, Yang Song (Huawei Technologies, China) "*HDTV1080p HEVC Intra Encoder with Source Texture Based CU/PU Mode Pre-decision*"

4C-4: Yi Liang, Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.) "*Fast Large-Scale Optimal Power Flow Analysis for Smart Grid through Network Reduction*"

4C-5: Cong Wang (Tsinghua Univ., China), Naehyuck Chang, Younghyun Kim, Sangyoung Park (Seoul National Univ., Republic of Korea), Yongpan Liu (Tsinghua Univ., China), Hyung Gyu Lee (Daegu Univ., Republic of Korea), Rong Luo, Huazhong Yang (Tsinghua Univ., China) "*Storage-Less and Converter-Less Maximum Power Point Tracking of Photovoltaic Cells for a Nonvolatile Microprocessor*"

Wednesday, January 22, 2014

Lunch Break (12:15 – 13:50)

13:50

5S: Special Session: Billion Chips of Trillion Transistors

Organizer: Chen-Yong Cher (IBM, U.S.A.)

5S-1: Chen-Yong Cher, K. Paul Muller, Ruud A. Haring, David L. Satterfield, Thomas E. Musta, Thomas M. Gooding, Kristan D. Davis, Marc B. Dombrowa, Gerard V. Kopcsay, Robert M. Senger, Yutaka Sugawara, Krishnan Sugavanam (IBM, U.S.A.) "*Soft Error Resiliency Characterization on IBM BlueGene/Q Processor*"

5S-2: Tanay Karnik, James Tschanz, Nitin Borkar, Jason Howard, Sriram Vangal, Vivek de, Shekhar Borkar (Intel, U.S.A.) "*Resiliency for Manycore System on a Chip*"

5S-3: Shahrzad Mirkhani (Univ. of Texas, U.S.A.), Hyungmin Cho, Subhasish Mitra (Stanford Univ., U.S.A.), Jacob Abraham (Univ. of Texas, U.S.A.) "*Rethinking Error Injection for Effective Resilience*"

5A: Simulation and Modeling

Chairs: Atushi Ike (Fujitsu, Japan), Yuichi Nakamura (NEC, Japan)

5A-1: Jun Ma, Guihai Yan, Yinhe Han, Xiaowei li (Chinese Academy of Sciences, China) "*Amphisbaena: Modeling Two Orthogonal Ways to Hunt on Heterogeneous Many-Cores*"

5A-2: Tomoyuki Nakabayashi, Tomoyuki Sugiyama, Takahiro Sasaki (Mie Univ., Japan), Eric Rotenberg (North Carolina State Univ., U.S.A.), Toshio Kondo (Mie Univ., Japan) "*Co-Simulation Framework for Streamlining Microprocessor Development on Standard ASIC Design Flow*"

5A-3: Rongjie Yan (State Key Laboratory of Computer Science, Institute of Software, China), De Ma (Hangzhou Dianzi Univ., China), Kai Huang, Xiaoxu Zhang, Siwen Xiu (Zhejiang Univ., China) "*Annotation and Analysis Combined Cache Modeling for Native Simulation*"

5A-4: Josef Schneider, Jorgen Peddersen, Sri Parameswaran (Univ. of New South Wales, Australia) "*A Scorchingly Fast FPGA-Based Precise L1 LRU Cache Simulator*"

5B: Reliability Analysis and Enhancement

Chair: Shigeki Nojima (Toshiba, Japan)

5B-1: Hsi-An Chien, Ting-Chi Wang (National Tsing Hua Univ., Taiwan) "*Redundant-Via-Aware ECO Routing*"

5B-2: Wei Wu, Fang Gong (Univ. of California, Los Angeles, U.S.A.), Gengsheng Chen (Fudan Univ., China), Lei He (Univ. of California, Los Angeles, U.S.A.) "*A Fast and Provably Bounded Failure Analysis of Memory Circuits in High Dimensions*"

5B-3: Deepashree Sengupta, Sachin Sapatnekar (Univ. of Minnesota, U.S.A.) "*Predicting Circuit Aging Using Ring Oscillators*"

5B-4: Ivan Ukhov, Mattias Villani, Petru Eles, Zebo Peng (Linköping Univ., Sweden) "*Statistical Analysis of Process Variation Based on Indirect Measurements for Electronic System Design*"

5C: Variational Design Techniques for Analog/Mixed-Signal Circuits

Chairs: C.Y. Tsui (Hong Kong Univ. of Science and Tech.), Hideki Asai (Shizuoka Univ., Japan)

5C-1: Jiandong Cheng, Guoyong Shi (Shanghai Jiao Tong Univ., China) "*Symbolic Computation of SNR for Variational Analysis of Sigma-Delta Modulator*"

5C-2: Yan Zhang, Sriram Sankaranarayanan, Fabio Somenzi (Univ. of Colorado, Boulder, U.S.A.) "*Sparse Statistical Model Inference for Analog Circuits under Process Variations*"

5C-3: Tan Yu, Sheldon Tan (Univ. of California, Riverside, U.S.A.), Yici Cai (Tsinghua Univ., China), Puying Tang (Univ. of Electronic Science and Tech. of China, China) "*Time-Domain Performance Bound Analysis for Analog and Interconnect Circuits Considering Process Variations*"

5C-4: Yang Song, Sai Manoj P. D., Hao Yu (Nanyang Technological Univ., Singapore) "*A Robustness Optimization of SRAM Dynamic Stability by Sensitivity-Based Reachability Analysis*"

15:30

Coffee Break (15:30 – 15:50)

Wednesday, January 22, 2014

15:50

6S: Special Session: Overcoming Major Silicon Bottlenecks: Variability, Reliability, Validation, and Debug (Tentative)

Organizer: Subhasish Mitra (Stanford Univ., U.S.A.)

6S-1: Liangzhen Lai, Puneet Gupta (UCLA, U.S.A.) "*Accurate and Inexpensive Performance Monitoring for Variability-Aware Systems*"

6S-2: Vikas Chandra (ARM, U.S.A.) "*Quantifying Workload Dependent Reliability in Embedded Processors*"

6S-3: David Lin, Subhasish Mitra (Stanford Univ., U.S.A.) "*QED Post-Silicon Validation and Debug: Frequently Asked Questions*"

6A: Synthesis of Quantum Circuits and Adaptive Logic

Chairs: Yusuke Matsunaga (Kyushu Univ., Japan), Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)

6A-1: Philipp Niemann, Robert Wille, Rolf Drechsler (Univ. of Bremen, Germany) "*Efficient Synthesis of Quantum Circuits Implementing Clifford Group Operations*"

6A-2: Robert Wille, Aaron Lye, Rolf Drechsler (Univ. of Bremen, Germany) "*Optimal SWAP Gate Insertion for Nearest Neighbor Quantum Circuits*"

6A-3: Alireza Shafaei, Mehdi Saeedi, Massoud Pedram (Univ. of Southern California, U.S.A.) "*Qubit Placement to Minimize Communication Overhead in 2D Quantum Architectures*"

6A-4: Sheng-Kai Wu, Po-Yi Hsu, Wai-Kei Mak (National Tsing Hua Univ., Taiwan) "*A Novel Wirelength-Driven Packing algorithm for FPGAs with Adaptive Logic Modules*"

6B: Contemporary Routing

Chairs: Mark Lin (National Chung Cheng Univ., Taiwan), Toshiyuki Shibuya (Fujitsu Labs., Japan)

6B-1: Po-Hsun Wu, Shang-Ya Bai, Tsung-Yi Ho (National Cheng Kung Univ., Taiwan) "*A Topology-Based ECO Routing Methodology for Mask Cost Minimization*"

6B-2: Yilin Zhang (Univ. of Texas, Austin, U.S.A.), Salim Chowdhury (Oracle, U.S.A.), David Z. Pan (Univ. of Texas, Austin, U.S.A.) "*BOB-Router: A New Buffering-Aware Global Router with Over-the-Block Routing Resources Optimization*"

6B-3: Meng-Ling Chen, Tu-Hsiung Tsai, Hung-Ming Chen (National Chiao Tung Univ., Taiwan), Shi-Hao Chen (Global Unichip, Taiwan) "*Routability-Driven Bump Assignment for Chip-Package Co-Design*"

6B-4: Zhongdong Qi, Yici Cai, Qiang Zhou (Tsinghua Univ., China), Zhuoyuan Li, Mike Chen (Nimbus Automation Technologies, China) "*VFGR: A Very Fast Parallel Global Router with Accurate Congestion Modeling*"

6C: Power Supply Noise Aware Design Optimization

Chairs: Wenjian Yu (Tsinghua Univ., China), Shi Guoyong (Shanghai Jiao Tong Univ., China)

6C-1: Ting Yu, Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.) "*Efficient Simulation-Based Optimization of Power Grid with On-Chip Voltage Regulator*"

6C-2: Ke Wang (Univ. of Virginia, U.S.A.), Brett Meyer (McGill Univ., Canada), Runjie Zhang, Kevin Skadron, Mircea Stan (Univ. of Virginia, U.S.A.) "*Walking Pads: Fast Power-Supply Pad-Placement Optimization*"

6C-3: Yuanqing Cheng (LIRMM, France), Aida Todri-Sanial (CNRS-LIRMM, France), Alberto Bosio (Univ. of Montpellier - LIRMM, France), Luigi Dilillo, Patrick Girard (CNRS-LIRMM, France), Arnaud Virazel (Univ. of Montpellier - LIRMM, France) "*Power Supply Noise-Aware Workload Assignments for Homogenous 3D MPSoCs with Thermal Consideration*"

6C-4: Xing Hu (Univ. of Chinese Academy of Sciences, China), Yi Xu (Advanced Micro Devices, China), Yu Hu (Univ. of Chinese Academy of Sciences, China), Yuan Xie (Advanced Micro Devices, China) "*SwimmingLane: A Composite Approach to Mitigate Voltage Droop Effects in 3D Power Delivery Network*"

17:30

Banquet & Banquet Keynote (18:30 – 21:00)

Chair: Masahiro Fujita (University of Tokyo, Japan)
Keynote: Ulf Schneider (Managing Director, Lantiq Asia Pacific Pte/President, SSIA, Singapore) "*The Art of Innovation - How Singapore Will Continue to Drive the Progress in Semiconductor Technologies*"

Thursday, January 23, 2014

Registration (08:00 –)

08:30 **3K: Keynote III**

Chair: Naehyuck Chang (Seoul National Univ., Republic of Korea)

09:30 Kaushik Roy (Purdue Univ., U.S.A.) "*Beyond Charge-Based Computing"*

Coffee Break (09:30 – 10:10)

10:10

7S: Special Session: Brain Like Computing: Modelling, Technology, and Architecture

Chair: Ahmed Hemani (KTH, Sweden)

7S-1: Anders Lansner, Ahmed Hemani, Nasim Farahini (KTH, Sweden) "*Spiking Brain Models: Computation, Memory and Communication Constraints for Custom Hardware Implementation*"

7S-2: Fabien Clermidy, Alexandre Valentian (CEA-LETI, France), Christian Gamrat, Olivier Bichler, Marc Duranton (CEA-LIST, France), Rodolphe Heliot (SCHNEIDER, France), Bilel Blehadj, Olivier Temam (INRIA, France) "*Advanced Technologies for Brain-Inspired Computing*"

7S-3: Kris Carlson, Michael Beyeler, Nikil Dutt, Jeff Krichmar (UC Irvine, U.S.A.) "*GPGPU Accelerated Simulation and Parameter Tuning for Neuromorphic Applications*"

7S-4: Nasim Farahini, Ahmed Hemani, Anders Lansner (KTH, Sweden), Fabian Clermidy (CEA-LETI, France), Christer Svensson (Linköping Univ., Sweden) "*A Scalable Custom Simulation Machine for the Bayesian Confidence Propagation Neural Network Model of the Brain*"

7A: Power and Life Time Issues of Memory Subsystem

Chairs: Muhammad Shafique (Karlsruhe Inst. of Tech., Germany), Wei Zhang (Nanyang Technological Univ.)

7A-1: Jia Zhan, Matt Poremba (Pennsylvania State Univ., U.S.A.), Yi Xu (AMD Research, China), Yuan Xie (The Pennsylvania State Univ. & AMD Research, U.S.A.) "*NoΔ:Leveraging Delta Compression for End-to-End Memory Access in NoC Based Multicores*"

7A-2: Jie Guo, Zhijie Chen (Univ. of Pittsburgh, U.S.A.), Danghui Wang (Northwestern Polytechnical Univ., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Yiran Chen (Univ. of Pittsburgh, U.S.A.) "*DPA: A Data Pattern Aware Error Prevention Technique for NAND Flash Lifetime Extension*"

7A-3: Venkata Kalyan Tavva, Ravi Kasha, Madhu Mutyam (Indian Inst. of Tech. - Madras, India) "*Scattered Refresh: An Alternative Refresh Mechanism to Reduce Refresh Cycle Time*"

7A-4: Chih-Yen Lai, Gung-Yu Pan, Hsien-Kai Kuo, Jing-Yang Jou (National Chiao Tung Univ., Taiwan) "*A Read-Write Aware DRAM Scheduling for Power Reduction in Multi-Core Systems*"

7A-5: Jianxing Wang, Yenni Tim, Weng-Fai Wong, Zhong-Liang Ong (National Univ. of Singapore, Singapore), Zhenyu Sun, Hai (Helen) Li (Univ. of Pittsburgh, U.S.A.) "*A Coherent Hybrid SRAM and STT-RAM L1 Cache Architecture for Shared Memory Multicores*"

7B: Advances in High-Level and Logic Synthesis

Chairs: Yuko Hara-Azumi (NAIST, Japan), Robert Wille (Univ. of Bremen, Germany)

7B-1: Benjamin Carrion Schafer (Hong Kong Polytechnic Univ., Hong Kong) "*Allocation of FPGA DSP-Macros in Multi-Process High-Level Synthesis Systems*"

7B-2: Preeti Ranjan Panda, Namita Sharma (Indian Inst. of Tech. Delhi, India), Arun Kumar Pilania, Gummidipudi Krishnaiah, Sreenivas Subramoney, Ashok Jagannathan (Intel Technology India Pvt., India) "*Array Scalarization in High Level Synthesis*"

7B-3: Luca Amaru, Pierre-Emmanuel Gaillardon (EPFL-LSI, Switzerland), Andreas Burg (EPFL-TCL, Switzerland), Giovanni De Micheli (EPFL-LSI, Switzerland) "*Data Compression via Logic Synthesis*"

7B-4: Nan Li, Elena Dubrova (Royal Inst. of Tech., Sweden) "*Synthesis of Power- and Area-Efficient Binary Machines for Incompletely Specified Sequences*"

7B-5: Min Li, Azadeh Davoodi (Univ. of Wisconsin - Madison, U.S.A.) "*Multi-Mode Trace Signal Selection for Post-Silicon Debug*"

7C: Advanced Test Solutions

Chairs: Jiun-Lang Huang (National Taiwan Univ., Taiwan), Mango Chia-Tso Chao (National Chiao Tung Univ.,Taiwan)

7C-1: Peter Waszecki, Matthias Kauer, Martin Lukasiewycz (TUM CREATE, Singapore), Samarjit Chakraborty (TU Munich, Germany) "*Implicit Intermittent Fault Detection in Distributed Systems*"

7C-2: Georgios Zervakis, Nikolaos Eftaxiopoulos, Kostas Tsoumanis, Nicholas Axelos, Kiamal Pekmestzi (National Technical Univ. of Athens (NTUA), Greece) "*A Segmentation-Based BISR Scheme*"

7C-3: Fu-Wei Chen, Hui-Ling Ting, TingTing Hwang (National Tsing Hua Univ., Taiwan) "*Fault-Tolerant TSV by Using Scan-Chain Test TSV*"

7C-4: Jerry C. Y. Ku, Ryan H.-M. Huang, Louis Y. -Z. Lin, Charles H.-P. Wen (National Chiao Tung Univ., Taiwan) "*Suppressing Test Inflation in Shared-Memory Parallel Automatic Test Pattern Generation*"

7C-5: Tsutomu Ishida, Izumi Nitta (Fujitsu Labs., Japan), Koji Banno (Fujitsu Semiconductor, Japan), Yuzi Kanazawa (Fujitsu Labs., Japan) "*A Volume Diagnosis Method for Identifying Systematic Faults in Lower-Yield Wafer Occurring during Mass Production*"

12:15

Thursday, January 23, 2014

Lunch Break (12:15 – 13:50)

13:50

8S: Special Session: Design Flow for Integrated Circuits using Magnetic Tunnel Junction Switched by Spin Orbit Torque

Organizer: Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany)

8S-1: Wang Kang, Weisheng Zhao, Zhaohao Wang, Jacques-Olivier Klein, Yue Zhang, Djaafar Chabi (IEF, Univ. Paris Sud, France), Youguang Zhang (Univ. Beihang, China), Dafiné Ravelosona, Claude Chappert (IEF, Univ. Paris Sud, France) "*An Overview of Spin-based Integrated Circuits*"

8S-2: Shunsuke Fukami, Hideo Sato, Michihiko Yamanouchi, Shoji Ikeda, Fumihiro Matsukura, Hideo Ohno (Tohoku Univ., Japan) "*Advances in spintronics devices for microelectronics - from spin-transfer torque to spin-orbit torque*"

8S-3: Gregory Di Pendina, Kotb Jabeur, Guillaume Prenat (SPINTEC - CNRS , CEA/DSM/INAC, France) "*Hybrid CMOS/Magnetic Process Design Kit and SOT-based Non-volatile Standard Cell Architectures*"

8S-4: Rajendra Bishnoi, Mojtaba Ebrahimi, Fabian Oboril, Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany) "*Architectural Aspects in Design and Analysis of SOT-based Memories*"

15:30

8A: Analysis, Optimization, and Scheduling for Multiprocessor Platforms

Chairs: Sebastian Steinhorst (TUM CREATE, Singapore), Akash Kumar (National Univ. of Singapore)

8A-1: Hardik Shah, Kai Huang, Alois Knoll (Technical Univ. Munich, Germany) "*Timing Anomalies in Multi-Core Architectures due to the Interference on the Shared Resources*"

8A-2: Karim Kanoun, David Atienza (École Polytechnique Fédérale de Lausanne, Switzerland), Nicholas Mastronarde (State Univ. of New York at Buffalo, U.S.A.), Mihaela van der Schaar (Univ. of California, Los Angeles (UCLA), U.S.A.) "*A Unified Online Directed Acyclic Graph Flow Manager for Multicore Schedulers*"

8A-3: Song Jin (North China Electric Power Univ., China), Yinhe Han (Chinese Academy of Sciences, China), Songwei Pei (Beijing Univ. of Chemical Tech., China) "*Variation-Aware Statistical Energy Optimization on Voltage-Frequency Island Based MPSoCs under Performance Yield Constraints*"

8A-4: Paula Aguilera, Katherine Morrow, Nam Sung Kim (Univ. of Wisconsin - Madison, U.S.A.) "*QoS-Aware Dynamic Resource Allocation for Spatial-Multitasking GPUs*"

8B: Advances in Formal Verification and Debugging

Chairs: Charles H.-P. Wen (National Chiao Tung Univ., Taiwan), Vishvender Singh (Infineon Technologies Asia-Pacific, Singapore)

8B-1: Brian Keng (Univ. of Toronto, Canada), Evean Qin (Vennsa Technologies, Canada), Andreas Veneris, Bao Le (Univ. of Toronto, Canada) "*Automated Debugging of Missing Assumptions*"

8B-2: Tobias Welp (UC Berkeley, U.S.A.), Andreas Kuehlmann (Coverity, U.S.A.) "*Property Directed Reachability for QF_BV with Mixed Type Atomic Reasoning Units*"

8B-3: Chien-Yu Lai, Cheng-Yin Wu, Chung-Yan (Ric) Huang (National Taiwan Univ., Taiwan) "*Adaptive Interpolation-Based Model Checking*"

8B-4: Miroslav Velev, Ping Gao (Aries Design Automation, U.S.A.) "*Efficient Parallel GPU Algorithms for BDD Manipulation*"

8C: Advances in CAD Techniques for Signal Integrity

Chairs: Rung-Bin Lin (Yuan Ze Univ., Taiwan), Sheldon Tan (Univ. of California, Riverside, U.S.A.)

8C-1: Chao Zhang, Wenjian Yu (Tsinghua Univ., China) "*Efficient Techniques for the Capacitance Extraction of Chip-Scale VLSI Interconnects Using Floating Random Walk Algorithm*"

8C-2: Qiaosha Zou, Dimin Niu, Yan Cao, Yuan Xie (Pennsylvania State Univ., U.S.A.) "*3DLAT: TSV-Based 3D ICs Crosstalk Minimization Utilizing Less Adjacent Transition Code*"

8C-3: Moning Zhang, Zuochang Ye (Tsinghua Univ., China) "*Tackling Close-to-Band Passivity Violations in Passive Macro-Modeling*"

8C-4: Takahiro Takasaki, Tadatoshi Sekine, Hideki Asai (Shizuoka Univ., Japan) "*HIE-Block Latency Insertion Method for Fast Transient Simulation of Nonuniform Multiconductor Transmission Lines*"

Coffee Break (15:30 – 15:50)

Thursday, January 23, 2014

15:50	**9S: Special Session: The Role of Photons in Harming or Increasing Security** Organizers: Francesco Regazzoni (Univ. of Lugano, Switzerland), Edorardo Charbon (Delft Univ. of Tech., Netherlands) **9S-1:** Juliane Krämer (Univ. Berlin), Michael Kasper (Fraunhofer Institute for Secure Information Technology, Germany), Jean-Pierre Seifert (Univ. Berlin) "*The Role of Photons in Cryptanalysis*" **9S-2:** Samuel Burri (EPFL, Switzerland), Damien Stucki (ID Quantique, Switzerland), Yuki Maruyama (Delft Univ. of Tech., Netherlands), Claudio Bruschini (EPFL, Switzerland), Edoardo Charbon (Delft Univ. of Tech., Netherlands), Francesco Regazzoni (ALaRI - USI, Switzerland) "*SPADs for Quantum Random Number Generators and Beyond*" **9S-3:** Mirko Lobino (Griffi • th Univ. and Univ. of Bristol, Australia), Anthony Laing (Univ. of Bristol, U.K.), Pei Zhang (Univ. of Bristol and Jiaotong Univ., U.K.), Kanin Aungskunsiri, Enrique Martin-Lopez (Univ. of Bristol, U.K.), Joachim Wabnig (Nokia Research Centre, U.K.), Richard W. Nock, Jack Munns, Damien Bonneau, Pisu Jiang (Univ. of Bristol, U.K.), Hong Wei Li (Nokia Research Centre, U.K.), John G. Rarity (Univ. of Bristol, U.K.), Antti O. Niskanen (Nokia Research Centre, U.K.), Mark G. Thompson, Jeremy L. O'Brien (Univ. of Bristol, U.K.) "*Quantum Key Distribution with Integrated Optics*"	**9A: System-Level Verification** Chair: Xiaowei Li (Inst. of Computing Tech., CAS, China) **9A-1:** Andreas Burger, Alexander Viehl, Andreas Braun (FZI Research Center for Information Technology, Germany), Finn Haedicke, Daniel Groβe (Solvertec, Germany), Oliver Bringmann, Wolfgang Rosenstiel (Univ. of Tübingen, Germany) "*Constraint-Based Platform Variants Specification for Early System Verification*" **9A-2:** Alexander Wolfgang Rath, Volkan Esen, Wolfgang Ecker (Infineon Technologies AG, Germany) "*A Transaction-Oriented UVM-Based Library for Verification of Analog Behavior*" **9A-3:** Matthias Kauer, Sebastian Steinhorst (TUM CREATE, Singapore), Reinhard Schneider (TU Munich, Germany), Martin Lukasiewycz (TUM CREATE, Singapore), Samarjit Chakraborty (TU Munich, Germany) "*Automata-Theoretic Modeling of Fixed-Priority Non-Preemptive Scheduling for Formal Timing Verification*"	**9B: Modeling and Evaluator for Emerging Technologies** Chairs: Guangyu Sun (Peking Univ., China), Wei Zhang (HKUST) **9B-1:** Shaodi Wang, Andrew Pan, Chi On Chui, Puneet Gupta (Univ. of California, Los Angeles, U.S.A.) "*PROCEED: A Pareto Optimization-Based Circuit-Level Evaluator for Emerging Devices*" **9B-2:** Cong Xu, Dimin Niu (Pennsylvania State Univ., U.S.A.), Shimeng Yu (Arizona State Univ., U.S.A.), Yuan Xie (Pennsylvania State Univ., U.S.A.) "*Modeling and Design Analysis of 3D Vertical Resistive Memory - A Low Cost Cross-Point Architecture*" **9B-3:** Miao Hu (Univ. of Pittsburgh, U.S.A.), Yu Wang (Tsinghua Univ., China), Qinru Qiu (Syracuse Univ., U.S.A.), Yiran Chen, Hai Li (Univ. of Pittsburgh, U.S.A.) "*The Stochastic Modeling of TiO2 Memristor and Its Usage in Neuromorphic System Design*" **9B-4:** Umamaheswara Rao Tida (Missouri Univ. of Science and Tech., U.S.A.), Cheng Zhuo (Intel research, U.S.A.), Yiyu Shi (Missouri Univ. of Science and Tech., U.S.A.) "*Through-Silicon-Via Inductor: Is It Real or Just A Fantasy?*"	**9C: Design and Simulation Toward Power and Temperature Awareness** Chair: Masanori Hashimoto (Osaka Univ., Japan), Yukihide Kohira (Univ. of Aizu, Japan) **9C-1:** Kimiyoshi Usami, Masaru Kudo, Kensaku Matsunaga, Tsubasa Kosaka, Yoshihiro Tsurui (Shibaura Inst. of Tech., Japan), Weihan Wang, Hideharu Amano (Keio Univ., Japan), Hiroaki Kobayashi, Ryuichi Sakamoto, Mitaro Namiki (Tokyo Univ. of Agri. and Tech., Japan), Masaaki Kondo (Univ. of Electro-Communications, Japan), Hiroshi Nakamura (Univ. of Tokyo, Japan) "*Design and Control Methodology for Fine Grain Power Gating Based on Energy Characterization and Code Profiling of Microprocessors*" **9C-2:** Yuan Liang, Wenjian Yu (Tsinghua Univ., China), Haifeng Qian (IBM, U.S.A.) "*A Hybrid Random Walk Algorithm for 3-D Thermal Analysis of Integrated Circuits*" **9C-3:** Smruti R. Sarangi, Gayathri Ananthanarayanan, M Balakrishnan (IIT Delhi, India) "*LightSim : A Leakage Aware Ultrafast Temperature Simulator*" **9C-4:** Wei Zhao, Yici Cai, Jianlei Yang (Tsinghua Univ., China) "*Fast Vectorless Power Grid Verification Using Maximum Voltage Drop Location Estimation*"
17:30				

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Registration

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FEES

Category	By Nov. 15, 2013 23:59 SIN time	From Nov. 16, 2013 To Jan. 19, 2014	Onsite
[Conference]			
*Member	S$750	S$850	S$900
Non-member	S$850	S$950	S$1000
Full-time Student	S$450	S$550	S$600

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Category	By Nov. 15, 2013 23:59 SIN time	From Nov. 16, 2013 To Jan. 19, 2014	Onsite
[Tutorial]			
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Non-member	S$330	S$400	S$400
Full-time Student	S$180	S$250	S$250
** Student Group	S$150	S$200	N.A.

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The conference fee includes:

- Admission to all sessions including keynote speeches except tutorials
- Banquet (excluding Full-time Students)
- One refreshment per break
- A conference kit (a final program and a set of conference proceedings)

The tutorial fee includes:

- Admission to tutorials
- Access to electronic files of tutorial presentations
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All registration fees must be paid in Singapore dollar (S$) by bank remittance or credit card. Please note that personal checks and bank drafts will not be accepted.

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When written notification of cancellation is received by the conference secretariat by December 19, 2013, 20% of paid costs will be deducted from the fees paid to cover administrative costs. No refunds will be made for cancellation requests received after this date. Speakers are not allowed to cancel registrations.

ON-SITE REGISTRATION HOURS (Suntec, Singapore)

Monday	January 20:	8:00 – 16:00
Tuesday	January 21	8:00 – 16:00
Wednesday	January 22	8:00 – 16:00
Thursday	January 23	8:00 – 16:00

Advance Registration Deadline: Nov. 15th, 2013

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Tutorial:
ASP-DAC has changed the format for the tutorials. Instead of full-day, in-depth tutorials, participants can choose two 3-hour tutorials – one in the morning session and one in the afternoon. For each session, four options are available – two in the physical-design domain and two in the system-design domain.

☐ **Tutorial** ☐ **No Tutorial**

"Student Group" discount is applied to a group of four or more students from the same affiliation (faculty or graduate school). One person should be chosen as a leader of the group. Please identify if you are the leader of the group or a member in the below.

☐ **Leader** ☐ **Member**

If you are the leader for your group (checked leader in Student Group), ASP-DAC 2014 Secretariat will ask you to submit a member list to confirm your members' registration later. After you receive an excel format file for the member list, please fill it out and send it back to aspdac2014-sec@mls.aspdac.com.

Registration Fee & Payment Method

Category	By Nov. 15, 2013 23:59 SIN time	From Nov. 16, 2013 To Jan. 19, 2014	Total
[Conference]			
Member	S$750	S$850	S$_____
Non-member	S$850	S$950	S$_____
Full-time Student	S$450	S$550	S$_____
[Tutorial]			
Member	S$280	S$350	S$_____
Non-member	S$330	S$400	S$_____
Full-time Student	S$180	S$250	S$_____
Student Group	S$150	S$200	S$_____
		Grand Total	S$_____

☐ **BANK TRANSFER**

I remitted or will remit a grand total of S$_____ on _____ (date/moth/year) through my bank named _____ to the following account:

Bank Name: OCBC Bank
(Oversea-Chinese Banking Corporation Bank)
Account Name: IEEE ASP-DAC 2014
Account No.: 514-771914-001

☐ **CREDIT CARD:**

☐ VISA ☐ MasterCard

Amount to be paid: S$_____

Card No.: _____-_____-_____-_____

Exp. Date: _____/_____ (month/year)

Cardholder's name: _____

Authorized Signature:

Date:_____ Signature: _____

Invoices and Receipts

Invoice Required? ☐ Yes ☐ No

If you replied "Yes", and you would like the invoice to be sent to a different address from that of your registration, please input the address below.

Invoice to

(name):_____

Address:_____

Receipt Required? ☐ Yes ☐ No

If you replied "Yes", and you would like the receipt to be sent to a different address from that of your registration, please input the address below.

Receipt to (name):_____

Address: _____

Note:

1. All payments must be in Singapore dollar (S$).
2. Bank drafts and personal checks will not be accepted.
3. If paying by credit card, please visit the Online Registration page (http://www.aspdac.com/) or send this form by post mail.
4. The remitter's name should be the same as the registrant's name.
5. If paying by bank transfer using your company's name, please advise us of the ID#, registrant's name, and transfer date (the day you transfer the fees) by e-mail to aspdac2014-sec@mls.aspdac.com. If you don't advise us above information within a week after you transfer the fee, we can't confirm your payment.
6. Handling fees and other bank transfer fees are to be borne by the registrant.
7. If payment of the registration fee is unremitted, or the credit card charge cannot be authorized, please go to the accounting desk.
8. If registered contents are changed or added, please notify the ASP-DAC 2014 Secretariat by e-mail at aspdac2014-sec@mls.aspdac.com. (Please be sure to specify your ID#.)
9. Cancellation and Refund.
   When you cancel this registration by December 19, 2013, regardless of reason, in refund, 20% of paid costs will be deducted from the fees paid to cover administrate cost. No refund will be made for cancellation request received after this date.
10. Speakers are not allowed to cancel registrations.

Attendee Survey

1. Which category best describes your work? (choose one only)
   - ( ) System or LSI Design
   - ( ) Research and Development of EDA Tools
   - ( ) Design Methodology
   - ( ) Marketing/Sales
   - ( ) Management
   - ( ) Research/Education in an Academic Institution
   - ( ) Student
   - ( ) Other

2. Which area do you primarily work in? (pick all that apply)
   - ( ) System Level ( ) Logic/Behavioral Level ( ) Circuit Level
   - ( ) Layout Level ( ) Process Technology Level
   - ( ) Design ( ) Design Methodology/Tool environment
   - ( ) Synthesis/Optimization ( ) Verification
   - ( ) Test
   - ( ) Embedded System ( ) Low Power
   - ( ) Timing and Signal Integrity ( ) Power Supply and Heat
   - ( ) Analog, RF, Mixed Signal ( ) System-level Integration, SIP
   - ( ) Other

3. What is your primary motivation/interest for attending ASP-DAC? (pick all that apply)
   - ( ) I am a speaker at the conference
   - ( ) I want to learn about EDA in general
   - ( ) I want to learn more about the basics of EDA
   - ( ) I want to learn more about advances in theory
   - ( ) I want to learn more about practical application of EDA
   - ( ) I have interest in Keynote speakers
   - ( ) I have interest in specific technical presentation(s)
   - ( ) I have interest in Special Sessions
   - ( ) I have interest in the technical program as a whole
   - ( ) I have interest in networking and social interaction opportunities
   - ( ) Other

4. How did you learn about ASP-DAC? (choose the two most significant factors)
   - ( ) ASP-DAC Website
   - ( ) E-mail
   - ( ) Previous Attendance
   - ( ) Colleague/Advisor
   - ( ) I have paper presentation at the conference
   - ( ) Other

Information

Proceedings:

ASP-DAC 2014 will be producing a set of the ASP-DAC 2014 Proceedings. Conference registration in any of the categories will include it. Additional Proceedings will be available for purchase at the Conference. Price is as follows:
Additional ASP-DAC 2014 Proceedings : S$30

Banquet:

Conference registrants are invited to attend a banquet to be held on January 22, 2014. The banquet will be held from 18:30 to 21:00 at Flower Field Hall, Gardens by the Bay. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students and Tutorial-only registrants wishing to attend the banquet will be required to pay **S$150 for a ticket** when they register on site.

Visa Application:

Most foreigners coming over to Singapore do not require a visa for entry. Please consult your local consular office for the latest travel information. The list of countries whose nationals require a visa to enter Singapore may be found in http://www.ica.gov.sg. Notice that the ASP-DAC 2014 Organizing Committee issues invitation letters and supports visa applications only for presenters of the conference papers. All the other attendees have to apply for a visa through their travel agents or by themselves. For requesting invitation letters, please contact Conference Secretariat (aspdac2014-sec@mls.aspdac.com).

Insurance:

The organizer will not accept responsibility for accidents which might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

Singapore has a tropical climate. Temperature ranges from a low of 24ºC to a high of around 31ºC every day, and relative humidity is high.

Currency Exchange:

Singapore dollar (S$) is accepted at stores and restaurants. You can exchange your currency for S$ at foreign exchange banks and authorized money exchange offices.

Electricity:

The electrical power supply is 230V at 50Hz. Three pin-sockets are the norm.

Shopping:

The business hours of most department stores are from 10:00 to 22:00. Department stores and most tourist attraction places are open 7 days a week.

Sightseeing:

You may browse the following website:
http://www.yoursingapore.com/content/traveller/en/experience.html

SENTOSA
Sentosa is a popular island resort in Singapore. Attractions include a 3.2km stretch of sandy white shores for different watersports, Imbiah Lookout – a cluster of attractions for adventure-seekers & nature lovers, Siloso Point – a home to many edutainment attractions, and the Resorts World Sentosa, featuring the theme park Universal Studios Singapore. For more information about Sentosa, please visit http://www.sentosa.com.sg/en/.

MARINA BAY
Marina Bay is a place for people for all walks of life to explore, exchange and entertain. Attractions nearby include an integrated resort – Marina Bay Sands, ArtScience Museum, Esplanade, Singapore Flyers, Gardens by the Bay, Merlion Park, etc. For more information about Marina Bay, please visit http://www.marina-bay.sg/attractions.html.

CHINA TOWN
China Town is an ethnic neighborhood featuring distinctly Chinese cultural elements. China Town is now an extremely vibrant place for shopping, walking around, sightseeing and eating. Be enjoyed in the China Town, with its stunning lights-up, night markets, decorations and various celebrations (especially before and after Chinese New Year). For visitors' information, the Chinese New Year 2014 will be on January 31, 2014.

ORCHARD ROAD
As a shopper's haven, Orchard Road is a swanky one-way boulevard flanked by distinctive and iconic shopping malls, restaurants and hotels. The shopping belt offers retail, dining and entertainment options to please any taste or budget - from opulent brands to high street fashion, and exclusive restaurants to fast food joints.

SINGAPAORE ZOO, NIGHT SAFARI, RIVER SAFARI, JURONG BIRD PARK
Singapore has several wildlife reserve attractions. These attractions are evolving from being "viewing" parks to "learning" parks, providing an experiential learning experience for visitors who will learn more about animals, birds, plants and the environment through sight/sounds, and to gain awareness on the need for conservation of wildlife. For more information, please visit http://www.wrs.com.sg/.

Other Information:

SINGAPORE CHANGI AIRPORT
http://www.changiairport.com/
SUNTEC INTERNATIONAL CONVENTION & EXHIBITION CENTRE
http://www.suntecsingapore.com
SINGAPORE TRANSPORTATION INFORMATION
http://www.smrt.com.sg/Home.aspx

Accommodations

HOTEL RESERVATION

All conference participants can book the hotel accommodation directly with the Hotel. Guest rooms are subjected to rooms' availability at the time of reservation. Please book earlier, preferably by **December 20, 2013**.

Hotels

No	Hotel Information
1	**Marina Mandarin, Singapore** (Tel: +65-6845-1188) Address: 6 Raffles Boulevard, Marina Square, Singapore 039594. Website: http://www.meritushotels.com/ Conference Room Rate (19 – 24 Jan. 2014)#: ▪ SGD $295++* per room per night ▪ Inclusive of one daily breakfast and complimentary internet access Book your Guest Room @: https://gc.synxis.com/rez.aspx?Hotel=23538&chain=9102&promo=ASP-DAC Getting to Suntec: 3-5 minutes walking distance
2	**Conrad Centennial Singapore** (Tel: +65-6334-8888) Address: 2 Temasek Boulevard, Singapore 038982. Website: http://conradhotels3.hilton.com Conference Room Rate (19 – 24 Jan. 2014)#: ▪ Classic Room – S$320++*/S$350++* (Single/Double) per room per night ▪ Business Room – S$360++*/S$390++* (Single/Double) per room per night ▪ Inclusive of one daily breakfast and room internet for 01 IP address Book your Guest Room: Visit http://www.ece.nus.edu.sg/stfpage/elehy/aspdac2014/hotel/index.html to download the Hotel Reservation Form, and complete and scan/email the Form to SINCICI.RES@conradhotels.com. Getting to Suntec: 3-5 minutes walking distance
3	**Hotel Grand Pacific** (Tel: +65-6336-0811) Address: 101 Victoria Street, Singapore 188018. Website: http://www.hotelgrandpacific.com.sg Conference Room Rate (19 – 24 Jan. 2014)#: ▪ Premier Room – S$195++*/S$210++* (Single/Twin) per room per night ▪ Inclusive of one daily breakfast and broadband internet Book your Guest Room: Visit http://www.ece.nus.edu.sg/stfpage/elehy/aspdac2014/hotel/index.html to download the Hotel Reservation Form, and complete and scan/email the Form to irene.sim@hotelgrandpacific.com.sg or fax the Form to +65-6334-0630. Getting to Suntec: 10 minutes walking distance from Bras Basah MRT[1].
4	**Hotel Royal @ Queens, Singapore** (Tel: +65-6725-9988) Address: 12 Queen, Singapore 188553. Website: http://www.royalqueens.com.sg Conference Room Rate (19 – 24 Jan. 2014)#: ▪ Executive Room – S$190++* (Single/Twin) per room per night ▪ Inclusive of one daily breakfast and broadband internet Book your Guest Room @: Visit http://www.ece.nus.edu.sg/stfpage/elehy/aspdac2014/hotel/index.html to find the online reservation link. Getting to Suntec: 100 meters from Bras Basah MRT[1].
5	**Oxford Hotel, Singapore** (Tel: +65-6332-2222) Address: 218 Queen Street, Singapore 188549. Website: http://www.oxfordhotel.com.sg/ Conference Room Rate (19 – 24 Jan. 2014)#: ▪ Premier Room – S$140++*/S$150++* (Single/Twin) per room per night ▪ Inclusive of one daily breakfast and wireless internet Book your Guest Room: Visit http://www.ece.nus.edu.sg/stfpage/elehy/aspdac2014/hotel/index.html to download the Hotel Reservation Form, and complete and scan/email the Form to sales@oxfordhotel.com.sg. Getting to Suntec: Walking distance from Bras Basah[1]/City Hall[2] MRT stations
6	**V Hotel Lavender** (Tel: +65-6345-2233) Address: 70 Jellicoe Road, Singapore 208767. Website: http://www.vhotel.sg/Lavender/ Conference Room Rate (19 – 24 Jan. 2014)#: ▪ Superior/Twin Room – S$138++* per room per night ▪ Triple Room – S$178++* per room per night ▪ Daily breakfast @ S$12++* per pax Book your Guest Room: Visit http://www.ece.nus.edu.sg/stfpage/elehy/aspdac2014/hotel/index.html to download the Hotel Reservation Form, and complete and scan/email the Form to seanchoo@vhotel.sg. Getting to Suntec: 7 minutes walking distance from Lavender MRT[2].
7	**Others** You may also book other hotels through the following websites at your own choice: http://www.openroomz.com/ http://www.asiatravel.com/ http://www.agoda.com.sg/ http://www.booking.com/ http://www.asiarooms.com/en/singapore/singapore.html

The conference rate does not apply to the reservation made directly on hotel website

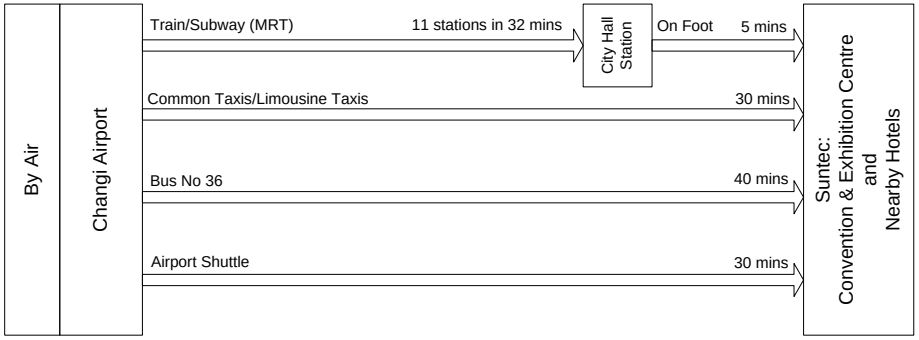
* Excluding 10% Service Charge and 7% Prevailing Goods & Services Tax

[1] Suntec is just above the Esplanade MRT station which is 1 station away from Bras Basah MRT station.

[2] Suntec is also near the City Hall MRT station which is 2 stations away from Lavender MRT station.

Access to Suntec, Singapore

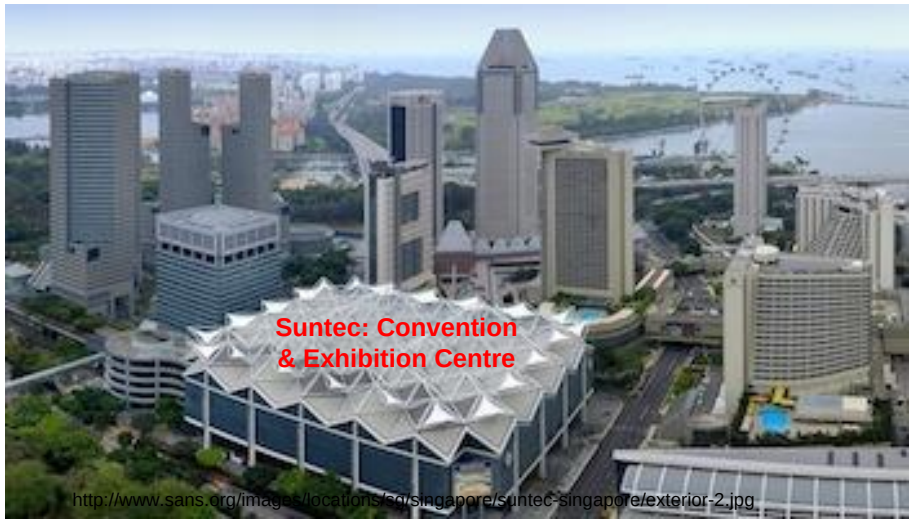
- Traffic information:



- Estimated cost (from Changi Airport to Suntec):
  - By Train/Subway (MRT): ~S$2
  - By Common Taxis: ~S$18 to ~S$38 depending on the sub-charges
  - By Limousine Taxis: ~S$55 to ~S$60
  - By Bus (no. 36): ~S$2
  - By Airport Shuttle: ~S$9

  More transportation information at Singapore Changi Airport, please visit http://www.changiairport.com/getting-around/to-and-from-the-airport.

- 2014 ASP-DAC Conference is held at Suntec Convention and Exhibition Center:



Visit our website
http://www.aspdac.com/

ASP-DAC 2014 SECRETARIAT
A'Tenga C. E.
2 Kallang Pudding Road,
#09-04 Mactech Industrial Building,
Singapore 349307
Email: aspdac2014-sec@mls.aspdac.com
Phone: +65-6746-4301
Fax: +65-6744-9342